PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

Do-Young KO

Docket No: Q54451

Appln. No.: 09/328,007

Group Art Unit: 2613

Confirmation No.:6191

Examiner: WONG, ALLEN C.

Filed: June 8, 1999

For: HORIZONTAL/VERTICAL SCANNING FREQUENCY CONVERTING APPARATUS IN MPEG DECODING BLOCK

SUBMISSION OF APPELLANT'S BRIEF ON APPEAL

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an original and two copies of Appellant's Brief on Appeal. A check for the statutory fee of $320.00 is attached. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

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Respectfully submitted,

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WASHINGTON OFFICE
23373
PATENT TRADEMARK OFFICE

Date: June 23, 2003

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REQUEST FOR ORAL HEARING

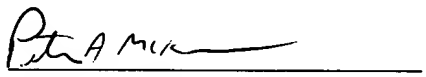
MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant hereby requests an Oral Hearing in the above-identified application before the Patent and Trademark Office Board of Patent Appeals and Interferences.

A check in the amount of $280.00 for requesting an Oral Hearing is attached. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this sheet is attached.

Respectfully submitted,



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APPELLANT'S BRIEF ON APPEAL UNDER 37 C.F.R. § 1.192

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 1.192, Appellant submits the following:

I. REAL PARTY IN INTEREST

The real party in interest is SAMSUNG ELECTRONICS CO., LTD, by virtue of an assignment executed by Do-young KO (Appellant, hereafter), on June 10, 1999, and recorded by the Assignment Branch of the U.S. Patent and Trademark Office on September 7, 1999 (at Reel 10220, Frame 0409).

II. RELATED APPEALS AND INTERFERENCES

To the knowledge and belief of Appellant, the Assignee, and the undersigned, there are no other appeals or interferences before the Board of Appeals and Interferences that will directly affect or be affected by the Board's decision in the instant Appeal.

III. STATUS OF CLAIMS

The application was originally filed with claims 1-5. Claims 1-5 are all of the claims currently pending in the application.

Claims 1-2 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by Song (U.S. Patent 5,539,467).

Claim 3 stands finally rejected under 35 U.S.C. § 103 as being unpatentable over Song in view of Richards (U.S. Patent 5,392,071).

Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

IV. STATUS OF AMENDMENTS

There are no outstanding amendments in this application.

V. SUMMARY OF THE INVENTION

The present invention relates to an apparatus for changing a horizontal/vertical scanning frequency in a decoding block for restoring an MPEG signal.

In an exemplary embodiment of the invention shown in Fig. 2, when I-picture data is received, the I-picture data is reverse quantized and reverse discrete cosine transformed in elements 201 and 202, respectively. The I -picture data is stored in the prediction memory 205 without being changed by adder 203. (Specification, page 5, line 29, to page 6, line 7.)

A P-picture is reversed discrete cosine transformed and input to the mixer 203 so that the error data of the P-picture is added to the data of the I-picture by the mixer 203 to obtain a forward prediction P-picture. The data of the forward predicted P-picture is stored in the second prediction memory 206 via the first switch 204. (Specification, page 6, lines 8-15.)

Then, the error data for bidirectionally predicting the B1-picture is input to the adder 203, and the I-picture stored in the first prediction memory 205 and the P-picture stored in the second prediction memory 206 are read and mean calculated by the mean operator 208. The mean operated data is output to the mixer 203 through the second switching unit 209, and the error data for the bi-directional prediction is added to the bi-directional mean calculated data. The bidirectionally predicted B1-picture is output from the mixer 203 and stored in the B-picture memory 207 via the first switching unit 204. (Specification, page 6, lines 15-26.)

When the B1-picture data is stored in the B-picture memory 207, the frequency of the read clock signal of the first and second prediction memories 205 and 206 and the B-picture memory 207 is set to be double that of the general scanning method. (Specification, page 6, lines 27-30.) Thus, the motion information transmitted from the transmitting side can be read twice as fast as in a general scanning method and the output can be twice as fast as the general scanning method.

In one embodiment of the invention shown in Fig. 4B, the field frequency can be double that of the general scanning method. Thus, it is possible to obtain a double scan converted output signal in which the vertical scanning frequency of the video signal is doubled. (Specification, page 7, lines 21-26.)

In another embodiment of the invention, a progressive scan converting operation for producing a horizontal scanning frequency which is twice that of the general scanning frequency method may also be achieved. (Specification, page 7, line 27, et seq.)

VI. ISSUES

The issues on appeal are:

1) Whether claims 1-2 are properly rejected under 35 U.S.C. § 102(b) as being anticipated by Song et al (U.S. Patent 5,539,467).

2) Whether claim 3 is properly rejected under 35 U.S.C. § 103 as being unpatentable over Song et al in view of Richards (U.S. Patent 5,392,071).

VII. GROUPING OF CLAIMS

For purposes of the present appeal, the rejected claims do not stand or fall together. Specifically, the rejected claims are divided into the following separately patentable groups.

Group 1: Claim 1.

Group 2: Claim 2.

Group 3: Claim 3.

VIII. ARGUMENTS

Appellant submits that claims 1-2 are not anticipated by Song et al, at least because this reference does not disclose the "B picture memory", recited in independent claim 1. Appellant submits that claim 3 is patentable over Song et al in view of Richards at least because these references, taken either alone or in combination, do not teach or suggest the claimed "B picture memory...."

In general, the operation of the present invention is significantly different from the operation of Song et al, at least in that the present invention stores B-picture data and reads out the B-picture data at an increased frequency. This enables the number of fields or lines displayed to be increased. On the other hand, Song et al stores I- and P-frame data and when B-frame data is introduced to the device, manipulates the stored I- and P-frame data and the received B-frame data to perform motion compensation in units of a half pixel. Song et al does not teach or suggest storing B pictures.

Summary of Song et al

Song et al relates to a B-frame processing apparatus including a motion compensation apparatus in units of a half pixel. According to one embodiment of Song et al, shown in Fig. 1 (reproduced below), when an I-frame is input, the I-frame data are inverse-quantized and IDCT-transformed by the restoring section 2 and then the restored data are stored in the first and third frame memories 12 and 24 (col. 8, lines 8-11). After this, when the first P-frame P1 enters, the P-frame data is added by the adder 23 to the value which is motion compensated by the first frame memory 12, and stored in the second and fourth frame memories 13 and 25 (col. 8, lines 11-16). When the first B-frame B1 enters, the value which is motion-compensated, respectively, by the first and second frame memories 12 and 13, is added by the adder 23 to the image signal inverse-quantized and IDCT-transformed (col. 8, lines 21-25). The added value is directly provided to the image processing section 28 through the slice buffer 27 without being stored in the frame memory (col. 8, lines 25-28). The next B-frame B2 is also provided to the image processing section 28 in the same way (col. 8, lines 28-29).

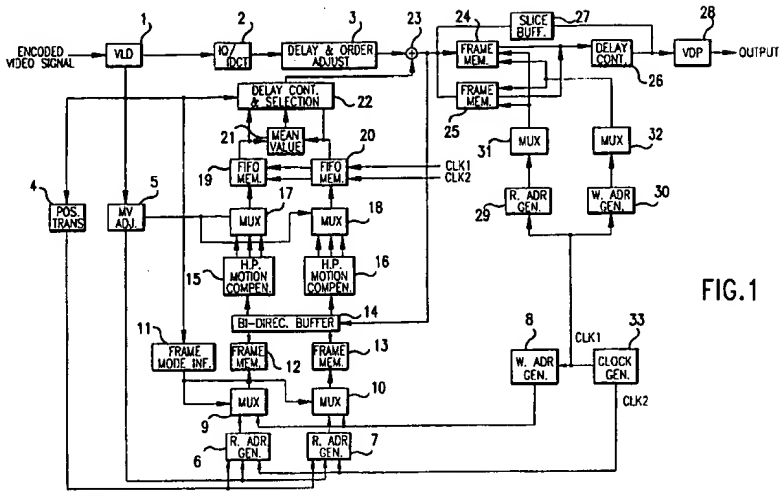


FIG.1

On the other hand, when the second P-frame P2 enters, the value which is motion-compensated by the second frame memory 13 is added by the adder 23 to the restored image data which has been inverse-quantized and IDCT-transformed, and then the added value is stored in the first and third frame memories 12 and 24 (col. 8, lines 30-36). At the same time, the data of the first P-frame P1 stored in the fourth memory 25 are read out and provided to the image processing section 28, thereby changing the display order of the image (col. 8, lines 36-39).

In another embodiment shown in Fig. 5 (reproduced below), when the I-frame enters, the image signal of the I-frame is stored in the first frame memory 45 through the adder 56 and the bi-directional latch 52 (col. 10, lines 3-5).

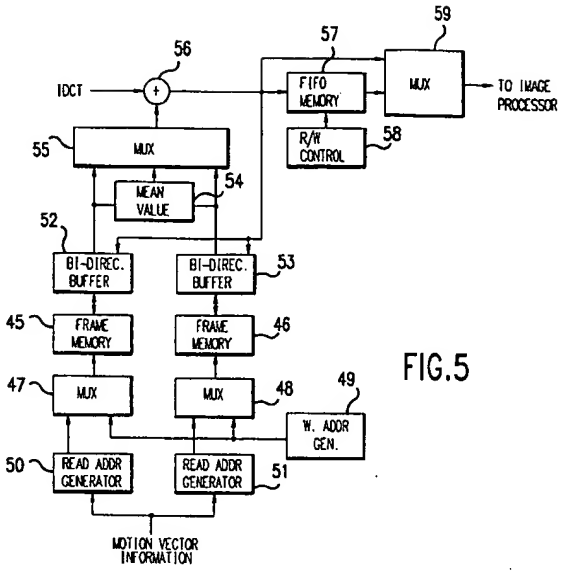


FIG.5

The write address of the first frame memory 45 is generated by the write address generator 49 (col. 10, lines 5-7). At this time, a data bus passes through the bi-directional latches 52 and 53, alternately with each frame and is stored in the respective frame memories, and the write address of the frame memory 46 corresponds to the address of the write address generator 49 (col. 10, lines 8-12). When the P1-frame enters, the I-frame image signal which has been previously stored is read out from the first frame memory 45 and enters the adder 56 through the bi-directional latch 52 and is added to the P1-frame image signal (col. 10, lines 18-22). The added video signal passes through the bi-directional latch 53 again and is stored in the second frame memory 46 (col. 10, lines 22-24). The read address of the first memory 45 may be generated by the first read address generator 50 utilizing motion vectors (col. 10, lines 24-26). The FIFO memory 57 can store the P1-frame image signal and provide an I-frame image signal at the same time (col. 10, lines 37-38). Thereafter, when the B1-frame enters, the frame

memories 45 and 46 stop the write operation and perform only image data read operation in accordance with read addresses provided from the read address generators 50 and 51 (col. 10, lines 39-43). The image data having been read in accordance with read addresses from the read address generators 50 and 51 whose input are motion vectors, are provided through the bi-directional buffers 52 and 53 and the provided image data are averaged by the mean value calculating section 54 (col. 10, lines 44-49). Multiplexor 55 provides the average image data, selectively to adder 56 (col. 10, lines 49-50).

Analysis of the Claim Rejections

In rejecting claim 1 as being anticipated by Song et al, the Examiner cites element 52 of Fig. 5 of Song et al as disclosing a B-picture memory for storing B-picture data, the B-picture data having been bidirectionally prediction restored by the decoding block. (Paper No. 9, p. 3, l. 11-12.)

Appellant submits, however, that element 52 of Fig. 5 is not a memory for storing B-picture data. In more detail, element 52 is a bi-directional latch for storing the image signal of the I-frame in the first memory 45 (col. 10, lines 3-5), and for outputting the image data of the stored I-frame from frame memory 45 when a B-frame is processed (col. 10, lines 37-49). Appellant has not identified any disclosure in Song et al that bi-directional buffer 52 is used to store a B-picture.

Appellant submits that claims 1-2 are not anticipated by Song et al, at least because this reference fails to teach the claimed B picture memory.

Appellant submits that claim 3 is not unpatentable over Song et al and Richards et al, at least because these references fail to teach or suggest the claimed B picture memory.

Arguments similar to those presented above were presented in Appellant's Response dated September 17, 2002. (Paper No. 8, p. 5.) In the Office Action dated November 26, 2002, the Examiner responded to those arguments by providing various reasons why he believes Song et al stores B-pictures (Paper No. 9, p. 2, numbered paragraph 2.). Each of these reasons will be addressed individually.

First, the Examiner states that his citation of Fig. 5, element 52 as a B picture memory is legitimate because B pictures must be stored, otherwise the display of all the MPEG encoded pictures would not be possible without storing all the I, P and B pictures. Appellant respectfully disagrees.

Song et al inputs pictures in the order I, P, B1, B2, P2, B3, B4, and P3, and outputs pictures in the order I, B1, B2, P1, B3, B4, and P2 (see, for example, the top and bottom lines of Figs. 4 and 6[1], reproduced below).

[1] Appellant notes that there is a typographical error in the bottom line of Fig. 6, where the entry "RP1" should be--B1--. RP1 means, "Read frame P1". Clearly, this is an incorrect notation for an output frame.

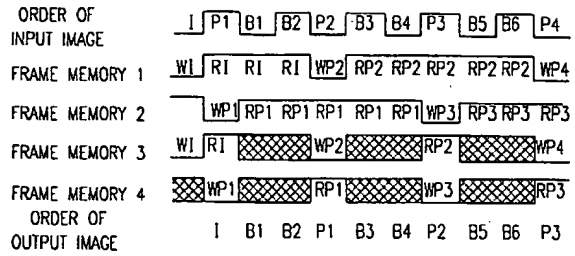


FIG.4

ORDER OF INPUT FRAME	I	P1	B1	B2	P2	B3	B4	P3
FRAME MEMORY 1	WI	RI	RI	RI	WP2	RP2	RP2	RP2
FRAME MEMORY 2		WP1	RP1	RP1	RP1	RP1	RP1	WP3
FIFO READ		RI			RP1			RP2
FIFO WRITE	WI	WP1			WP2			WP3
ORDER OF OUTPUT IMAGE		I	RP1	B2	P1	B3	B4	P2

FIG.6

Accordingly, there is no need to store B pictures. For example, when the B1 frame is input to adder 56 of Fig. 5, the B1 data is added to the data of the I frame stored in frame memory 1 (element 45) and/or the P1 frame stored in frame memory 2 (element 46). The data output by adder 56 is directly applied to multiplexor 59 for outputting to the image processor. That is, when the B1 frame data is input, B1 frame data is output at the same time, as shown in the charts of Figs. 4 and 6. It is not necessary that the B pictures be stored; and it is not suggested that the B-frame is stored. Inspection of Fig. 4 shows that while I-frames and P-frames are stored (WI, WP1, WP2, WP3, that is write I frame, write frame P1, write frame P2, write frame P3, write frame P4, respectively) the B frames are not stored (that is, there is no WB1 or WB2, etc.). Furthermore, comparison of the top line of Fig. 4 ("ORDER OF INPUT

IMAGE") and the bottom line of Fig. 4 ("ORDER OF OUTPUT IMAGE"), shows that the B1 frame is output at the same time the B1 frame is input, the B2 frame is output at the same time the B2 frame is input, the B3 frame is output at the same time the B3 frame is input, and so forth. As is made clear from these figures, the B frames are not stored.

Second, the Examiner states that Song's Fig. 5, element 52 is a bi-directional latch for a temporary storage unit for temporarily storing bi-directional pictures. Appellant respectfully disagrees that element 52 temporarily stores bi-directional pictures. Rather, the bi-directional latches 52 and 53 merely allow the passage of data in two directions. This is an entirely different concept from storing the bi-directional picture (that is, B picture) of the MPEG system, where a bi-directional picture is coded/encoded with respect to previous and future pictures (that is, with respect to two temporal directions). The data flow into and out of element 52 is described at col. 10, lines 3-64. It is described that I-frame data and P-frame data is stored, but there is no description that B-frame data is stored. Fig. 6, which is a timing diagram for certain elements of the Fig. 5 embodiment, does not indicate that a B-frame is stored. On the contrary, the top and bottom lines of Fig. 6 clearly indicate that B-frames are output at the same time they are input (keeping in mind that the bottom line of Fig. 6 contains a typographical error, where "RP1" should be --B1--).

The Examiner further states that in Song's Fig. 5, element 55 can produce the B-frame image data and send it to element 57, a FIFO memory or a first-in-first-out memory for temporarily storing the B-frame image date before displaying the MPEG decoded pictures.

Appellant respectfully disagrees with the Examiner's analysis because there is no teaching or suggestion in Song et al that the FIFO memory 57 of Fig. 5 stores a B-frame. As shown in the timing diagram of Fig. 6, FIFO writes only the I-frame, the P1-frame, the P2-frame, and the P3-frame. Further, as explained above, Fig. 6 indicates that B-frame data is output at the same time that it is input. This is consistent with the explanation of the operation of the Fig. 5 device in col. 10 of Song et al.

Lastly, the Examiner states that element 79 of Fig. 7 is also considered a B-frame buffer that stores a B-frame signal. Appellant submits that element 79 is not a buffer used for storing data. Generally, there are several types of buffers used in electronic circuits: a first type of buffer is an amplifier used to isolate one stage of circuitry from a succeeding stage; a second type of buffer is a storage site for temporarily storing data to compensate for difference in data flow rates. Definitions for each of these types of buffer are given, for example, on page 77 of "The Illustrated Dictionary of Electronics", a copy of which is provided. Element 79 is the first type of buffer. That is, element 79 serves to isolate the adder 76 from the line feeding the image processor. That element 79 is the first type of buffer is shown by its symbol (see Fig. 7, reproduced below). The first type of buffer is described in detail on pages 424-425 of the book "Fundamentals of Logic Design". Enclosed are pages 424 and 425 which describe the 3-state buffer which is used as an interface between two circuits, but does not act to store data. Appellant submits that the Examiner is ascribing features of the second type of buffer (that is, the data storage type of buffer) to element 79, which is an isolating buffer.

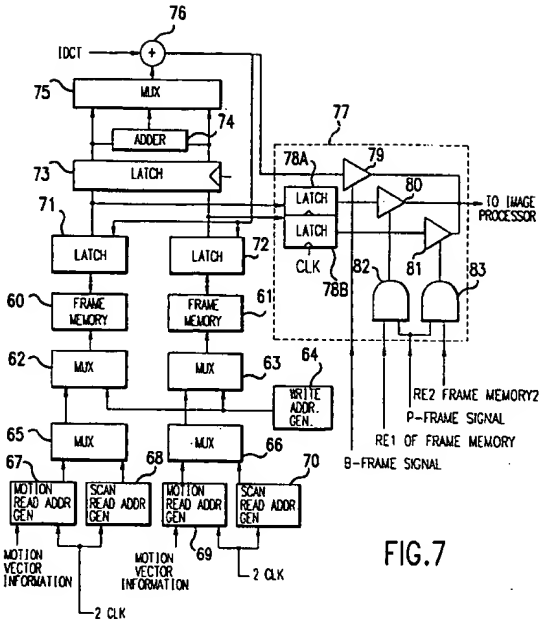


FIG.7

Arguments similar to those presented above were included in the Response filed by Appellant on February 24, 2003 (Paper No. 10). In the Advisory Action dated March 11, 2003, the Examiner mentions each of the above arguments, but does not generally reply to the specific points raised in the arguments. Instead, for many of the points raised above, the Advisory Action simply repeats earlier positions taken by the Examiner. There are, however, certain new points which the Examiner has raised.

First, the Examiner states, "Again, as mentioned above, Song's fig. 5, element 52 does not merely allow the passage of data, it also temporarily stores data, otherwise data would be lost." (Paper No. 11, p. 2, lines 11-12.) Appellant does not dispute that element 52 stores data. Rather, Appellant submits that element 52 does not store B picture data. As explained above,

Song et al does not store B picture data, but instead outputs B picture data as it is received (see Fig. 6).

Second, the Examiner states, "Lastly, on the bottom of page 3 of applicant's remarks, applicant sates that Song's fig. 7, element 79 does not act to store data. The Examiner respectfully disagrees. A perusal of Song's fig. 7 shows that 'B-frame signal' goes to buffer or memory element 79." (Paper No. 9, p. 2, lines 12-14.) In response, Appellant submits that the buffer 79 is not a memory element. Element 79 is merely a three-state buffer such as described on pages 424-425 of the book "Fundamentals of Logic Design", wherein "when the buffer 79 is enabled by the B-frame signal, the adder 76 provides a B-frame image signal to the image processing section" (Song et al, col. 13, lines 26-28). The Examiner has attributed features of the second type of buffer (that is, the storage-type buffer) to element 79, which is an isolation-type buffer.

With respect to the grouping of claims, Appellant submits that claim 2 is separately patentable from claim 1. One reason for this is that claim 2 recites that "the period of a data read is reduced to half by setting read clock frequencies of the prediction memory and the B picture memory to be two times higher than the read clock frequencies of a general scanning method." Appellant submits that this feature is not disclosed by Song et al. In rejecting claim 2, the Examiner states that Song et al, at col. 12, lines 7-12, discloses that the memory data read is reduced by half. However, this portion of Song et al relates to the speed at which data is read from frame memories 60 and 61. Since these memories do not store B-frames, Appellant

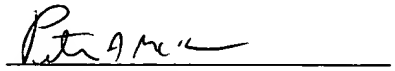
submits that this portion of Song et al does not disclose the feature of claim 2 whereby the read clock frequencies of the B-picture is set to be two times higher than the that of a general scanning method.

With respect to claim 3, Appellant submits that claim 3 is separately patentable from claims 1 and 2. One reason for this is that Song et al does not disclose the feature of claim 3, "wherein the output data switching portion performs switching control so as to double the vertical scanning frequency of a video signal by repeating output data twice in units of a picture with respect to a general scanning method." Since the Examiner notes, in rejecting claim 3, that "Song does not disclose the doubling of the vertical scanning frequency", Appellant believes that no further reasons need to be advanced regarding this issue.

The present Brief on Appeal is being filed in triplicate. Unless a check is submitted herewith for the fee required under 37 C.F.R. §1.192(a) and 1.17(c), please charge said fee to Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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23373
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Date: June 23, 2003

APPENDIX

CLAIMS 1-5:

1. An apparatus for changing a horizontal\vertical scanning frequency in a decoding block for restoring an MPEG signal including a prediction memory for storing I picture data and forward prediction restored P picture data and a mean operating unit for generating calculated mean data for bidirectional prediction, comprising:

a B picture memory for storing B picture data, the B picture data having been bidirectionally prediction restored by the decoding block;

a prediction memory switching portion for switching data output from the decoding block to the prediction memory or the B picture memory depending on the type of picture; and

an output data switching portion for increasing the switching frequency of data stored in the prediction memory and the B picture memory with respect to a general scanning method, using the motion vector of the decoding block, and outputting the converted data.

2. The apparatus of claim 1, wherein the period of a data read is reduced to half by setting read clock frequencies of the prediction memory and the B picture memory to be two times higher than the read clock frequencies of a general scanning method.

3. The apparatus of claim 1, wherein the output data switching portion performs switching control so as to double the vertical scanning frequency of a video signal by repeating output data twice in units of a picture with respect to a general scanning method.

4. The apparatus of claim 1, wherein the output data switching portion performs switching control so as to repeat data of a corresponding horizontal line of a previous picture

between horizontal lines of a picture when the value of a motion vector is no more than a reference value and to insert corresponding line data of a previous picture stored in the prediction memory between the horizontal lines of the picture when the value of the motion vector is larger than the reference value.

5. The apparatus of claim 1, wherein the output data switching portion performs switching control so as to repeat the data of a corresponding horizontal line of a previous picture between horizontal lines of a picture when the value of a motion vector is no more than a reference value and to insert the calculated line mean data of the mean operating portion between the horizontal lines of the picture when the value of the motion vector is larger than the reference value.